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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,403	11/19/2003	Patrick Y. Huct	58551.US	8656
60838	7590	10/19/2007	EXAMINER	
LNG/KLA JOINT CUSTOMER C/O LUEDEKA, NEELY & GRAHAM, P.C. P.O. BOX 1871 KNOXVILLE, TN 37901			VALENTIN, JUAN D	
		ART UNIT	PAPER NUMBER	
		2877		
		MAIL DATE		DELIVERY MODE
		10/19/2007		PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/717,403	HUET ET AL.
	Examiner Juan D. Valentin II	Art Unit 2877

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 26 July 2007.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.  
 4a) Of the above claim(s) 6-20 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-5 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 07/26/2007 have been fully considered but they are not persuasive. Applicant has argued that Examiner has not made a *prima facia* case of obviousness in regards to the rejections of claims 1-5. Examiner kindly disagrees with applicant's assertions. Naya et al. (2001/0021019, hereinafter Naya) in [0003] discloses:

"A semiconductor device is formed by repeating a step of transferring a circuit pattern formed on a photomask to a semiconductor wafer by a lithographing process and an etching process. A state of the process, the presence or absence of generation of a foreign matter (particles), and the like in the manufacturing step of the semiconductor device largely exercise an influence on a manufacturing yield of the semiconductor device. To detect them early or preparatorily, a method of inspecting the circuit pattern of the semiconductor wafer in the manufacturing step of the semiconductor device has conventionally been used." (emphasis added)

Examiner has previously stated that the logical division of a wafer in different inspection sections is well known and obvious to one of ordinary skill in the art. If there is a plurality of dies (circuit patterns) located on a wafer, then each die will be inspected separately from one another just as they were manufactured on the wafer, they will be inspected in a similar manner as indicated by Naya above. As for step B), it is well within the knowledge of anyone of ordinary skill in the art at the time of the claimed invention that if one carrying out defect inspection as disclosed by Naya above, then once a defect is detected, then some form of information regarding that defect must be present after detection even if the only information about said defect is its location. Further, the classification of defects within separate zones or dies on a semiconductor wafer is neither unique nor novel as previously indicated by examiner. It is

obvious that when inspecting a semiconductor wafer, some form of an analysis method will be used. Further as previously indicated by examiner with regards to claims 3-4, the use of well known and appropriate analysis methods would have been obvious and it does not appear to be disclosed sufficiently in the specification to indicate or support that the claimed analysis methods are created by the current inventors as the first and original inventors to use these methods in the inspection of semiconductor wafers. Applicant has not indicated as much in the reply to the Non-Final Office action dated 05/30/2007. Applicant further claims to “logically divide” a wafer into “zones” after the substrate has been inspected. As previously indicated by examiner, this “logical” division would be an obvious and no pun intended, but a logical step to one of ordinary skill in the art when creating a recipe or inspection map to be carried out.

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nara et al (US 2001/0021019).

Naya et al shows inspecting and analyzing defect information on a substrate. The substrate being inspected has thereon a plurality of circuit patterns (see paragraph [0003]), and part of the inspection the substrate is “logically dividing the substrate in to zones” (the various individual circuits). As in claim 2, the reference describes inspecting the individual circuits and

classifying the defects found therein; this inspection and classification must be done by some “analysis method”. As in claims 3 and 4, the method is shown as a computer, so it is at least obvious to use a “recipe”. The use of known appropriate analysis methods would have been obvious; it does not appear that the specification presents, nor does it appear that applicant is alleging, to be the first and original inventors of the different methods of claims 3 and 4, nor does there appear to be disclosure sufficient to support such an allegation in the instant specification. As in claim 5, using image analysis software to “logically divide” the scanned data in to the appropriate “zones” would have been obvious; this would have the benefit of allowing the inspection apparatus to be easily configured to different substrates with different patterns that may be, for example, different sizes.

### *Conclusion*

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Su et al. discloses a process for measuring the location of the CD of a mask pattern on a series of dies located within a semiconductor wafer (abstract).

Ebert et al. discloses identifying a series of measurement sites within a wafer (creating a measurement recipe), moving the imaging system from measurement site to measurement site performing a wafer inspection (entire patent).

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

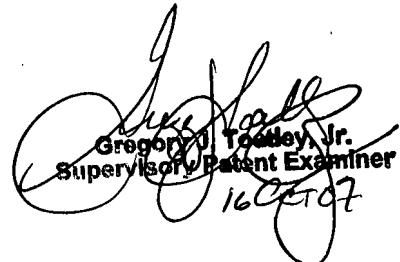
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan D. Valentin II whose telephone number is (571) 272-2433. The examiner can normally be reached on Mon.-Fri..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory J. Toatley, Jr. can be reached on (571) 272-2800 ext. 77. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JDVII/  
Juan D Valentin II  
Examiner 2877  
JDV



Gregory J. Toddy, Jr.  
Supervisory Patent Examiner  
16 OCT 07